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APPLICATION NUMBER	FILING DATE	FIRST NAMED APPLICANT	ATTORNEY DOCKET NO.

EXAMINER	
ART UNIT	PAPER NUMBER
	16

DATE MAILED:

This is a communication from the examiner in charge of your application
COMMISSIONER OF PATENTS AND TRADEMARKS

OFFICE ACTION SUMMARY

☒ Responsive to communication(s) filed on 12/5/97 & 3/27/98

This action is **FINAL**.

Since this application is in condition for allowance except for formal matters, **prosecution as to the merits is closed** in accordance with the practice under *Ex parte Quayle*, 1935 D.C. 11; 453 O.G. 213.

A shortened statutory period for response to this action is set to expire 3 month(s), or thirty days, whichever is longer, from the mailing date of this communication. Failure to respond within the period for response will cause the application to become abandoned. (35 U.S.C. § 133). Extensions of time may be obtained under the provisions of 37 CFR 1.136(a).

Disposition of Claims

☒ Claim(s) 1-27 is/are pending in the application.

Of the above, claim(s) 1-5, 11-17, 20-21, 24, 27 is/are withdrawn from consideration.

Claim(s) _____ is/are allowed.

☒ Claim(s) 6-10, 18-19, 22-23 and 25-26 is/are rejected.

Claim(s) _____ is/are objected to.

Claims _____ are subject to restriction or election requirement.

Application Papers

See the attached Notice of Draftsperson's Patent Drawing Review, PTO-948.

The drawing(s) filed on _____ is/are objected to by the Examiner.

The proposed drawing correction, filed on _____ is approved disapproved.

The specification is objected to by the Examiner.

The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. § 119

Acknowledgement is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d).

All Some* None of the CERTIFIED copies of the priority documents have been

received.

received in Application No. (Series Code/Serial Number) _____

received in this national stage application from the International Bureau (PCT Rule 17.2(a)).

*Certified copies not received: _____

Acknowledgement is made of a claim for domestic priority under 35 U.S.C. § 119(e).

Attachment(s)

Notice of Reference Cited, PTO-892

Information Disclosure Statement(s), PTO-1449, Paper No(s).

Interview Summary, PTO-413

Notice of Draftsperson's Patent Drawing Review, PTO-948

Notice of Informal Patent Application, PTO-152

-- SEE OFFICE ACTION ON THE FOLLOWING PAGES --

Claims 1-27 are pending in this application. Claims 1-5, 11-17, 20-21, 24, and 27 stand withdrawn from further consideration by the examiner.

In view of the appeal brief filed on 4/6/98, PROSECUTION IS HEREBY REOPENED. New grounds of rejection are set forth below.

To avoid abandonment of the application, appellant must exercise one of the following two options:

(a) file a reply under 37 CFR 1.111 (if this Office action is non-final) or a reply under 37 CFR 1.113 (if this Office action is final); or,

(b) request reinstatement of the appeal.

If reinstatement of the appeal is requested, such request must be accompanied by a supplemental appeal brief, but no new amendments, affidavits (37 CFR 1.130, 1.131 or 1.132) or other evidence are permitted. See 37 CFR 1.193(b)(2).

The following is a quotation of the first paragraph of 35 U.S.C. 112:

> The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

Claims 6-8, 18-19, 22-23, and 25-26 are rejected under 35 U.S.C. 112, first paragraph, because the specification, while being enabling for structures formed through the use of applicant's disclosed improved techniques and resultant structures (*e.g.* applicant's bird's beak reduction, increased storage node capacitance, at least five conductive lines, elimination of field

oxide techniques, etc), does not reasonably provide enablement for memory structures having the claimed density not made through at least one of applicant's improved techniques. The specification does not enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make the invention commensurate in scope with these claims.

> "*Maximizing density of single transistor and other memory cells is a continuing goal in semiconductor memory fabrication.*"[1]

Between this phrase and applicant's all-encompassing claims, applicant discloses several methods and their resultant structures which allow applicant to produce the claimed device having improved memory cell density. None of these methods, or any of their corresponding structural manifestations, are recited in the rejected claims. Instead, applicant's claims are written in terms of maximum device density. As such, the scope of applicant's claims includes all devices having the density achieved by applicant as well as all future improvements in density, made through any means, known or unknown. The Federal Circuit has repeatedly held that "the specification must teach those skilled in the art how to make and use the full scope of the claimed invention without 'undue experimentation'." *In re Wright*, 27 USPQ2d 1510, 1513 (Fed. Cir. 1993). With respect to the breadth of a claim relevant to enablement, the dispositive issue is whether the scope of enablement provided to one skilled in the art by the disclosure is commensurate with the scope of the protection sought by the claims. *In re Moore*, 169 USPQ 236, 239 (CCPA 1971).

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[1]Specification, page 2, lines 7-8.

> "The determination of the propriety of a rejection based upon the scope of a claim relative to the scope of the enablement involves two stages of inquiry. The first is to determine how broad the claim is with respect to the disclosure. The entire claim must be considered. The second inquiry is to determine if one skilled in the art is enabled to make and use the entire scope of the claimed invention without undue experimentation."[2]

The scope of applicant's claims includes all semiconductor memory devices of the type claimed, having memory cell density equal to or greater than that achieved by applicant and made through any means at all. Given that maximizing density of memory cells is a continuing goal in semiconductor fabrication as well as the apparent novelty of applicant's claimed structure, it would appear that the semiconductor industry has been unable to produce applicant's claimed structure despite a continuing goal to do so. The examiner maintains that what has stood in the way of achieving this goal is the lack of successful manufacturing techniques and structural features which allow for the production of devices having the density achieved by applicant. As such, applicant's disclosure enables one skilled in the art to make the claimed invention only through the use of applicant's disclosed processing techniques and their structural details.

Applicant's acknowledgment of an industry goal to increase the density of memory devices combined with the disclosure's frequent statement that methods other than those described could be used to form the claimed structure falls far short of enabling one skilled in the art to make the claimed invention through the use of an undisclosed method. The examiner

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[2]MPEP 2164.08.

maintains that the ability to make the claimed invention through the use of a method other than those disclosed is not within the level of ordinary skill in the art.

Applicant may be entitled to a patent because no prior artisan has been able to produce the device produced by applicant. However, applicant's claims may not be so broad so as to include within their scope devices which are not enabled by applicant's disclosure. Applicant's disclosure is enabling only for devices made through the use of the disclosed methods and including the disclosed structural features of these methods.

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 6-10, 18-19, 22-23, and 25-26 are rejected under 35 U.S.C. 103(a) as being unpatentable over applicant's discussion of the prior art in view of Denboer ("Inside Today's Leading Edge Microprocessors," Semiconductor International, 2/1994).

In applicant's "BACKGROUND OF THE INVENTION," applicant discloses that 16M DRAM chips exist in the prior art (page 2, line 15), that DRAM chips are normally made with cells arranged in multiple repeating memory arrays, and that "[m]aximizing density of single transistor and other memory cells is a continuing goal in semiconductor memory fabrication." (page 2, lines 7-8) Denboer further discusses the goal of minimizing device size and discusses a

structure which achieves a small size and uses 5 conductive layers (note page 2, middle col.) Applicant's claims are written in terms of total combined area of the memory cells or total combined area of the peripheral and pitch circuitry as well as the memory cells. It would have been obvious to one skilled in the art at the time the invention was made to make 16M DRAM chips with ever increasing device density because, as applicant admits, 16M DRAM chips existed in the prior art at the time of invention and because maximizing density of single transistors and other memory cells is a continuing goal in the art. Furthermore, since applicant discloses that one way to achieve the claimed structure is through the use of at least 5 conductive layers and since Denboer teaches the known use of such a structure, the examiner maintains that one skilled in the art would be able to produce the claimed structure.

Applicant's disclosure of the prior art fails to discuss a package having an encapsulating body and electrically conductive interconnect pins extending outwardly from the body, the specific number of cells per array, and the particular number of conductive layers used in the prior art. With respect to the claimed package, such packages are well known to those skilled in the art. With respect to the specific number of cells per array, this number is a function of overall device design and the use of any particular number of cells per array would have been obvious to one skilled in the art at the time of invention depending upon specific device architecture. Finally, with respect to the number of conductive lines used (a feature which is disclosed by applicant as one which enables production of a structure having the recited density), one skilled in the art would have known at the time the invention was made that semiconductor devices may be

fabricated with fewer than, or more than, four conductive layers, as shown by Denboer (figures 1 and 6), depending on particular device design. It would have been obvious to one skilled in the art at the time the invention was made to encapsulate the claimed memory device in a package as recited, to form the arrays with the particular number of cells as claimed, and to include less than four, or more than four, conductive line layers because all these variations are known to those skilled in the art and would have resulted from routine engineering design, optimization, and implementation considerations.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Nathan Kelley whose telephone number is (703) 305-3789. The fax phone number for this Group is (703) 308-7722.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the Group receptionist whose telephone number is (703) 308-0956.

Olik Chaudhuri
Supervisory Patent Examiner
Technology Sector 2800

N. Kelley
June 18, 1998